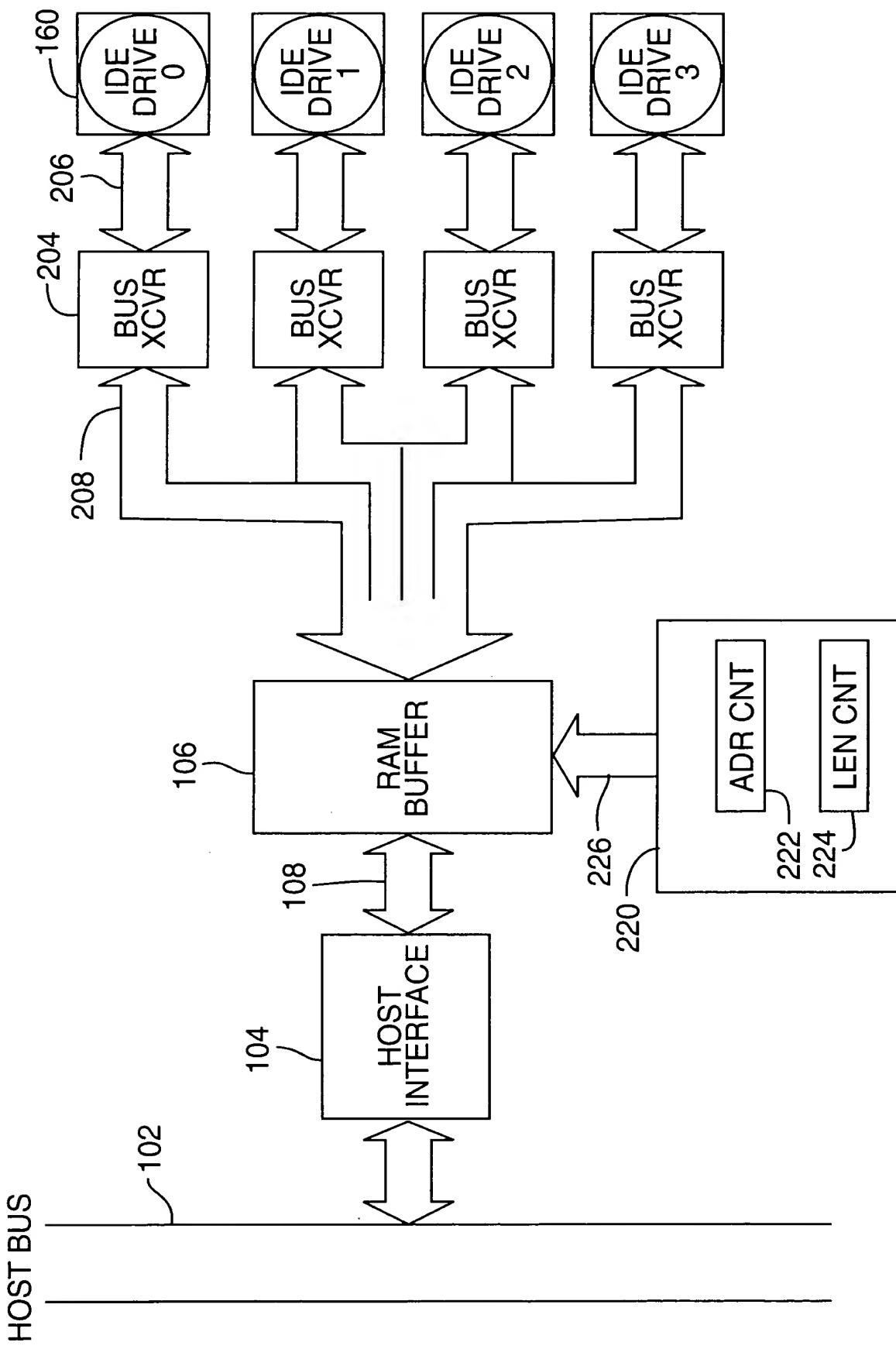
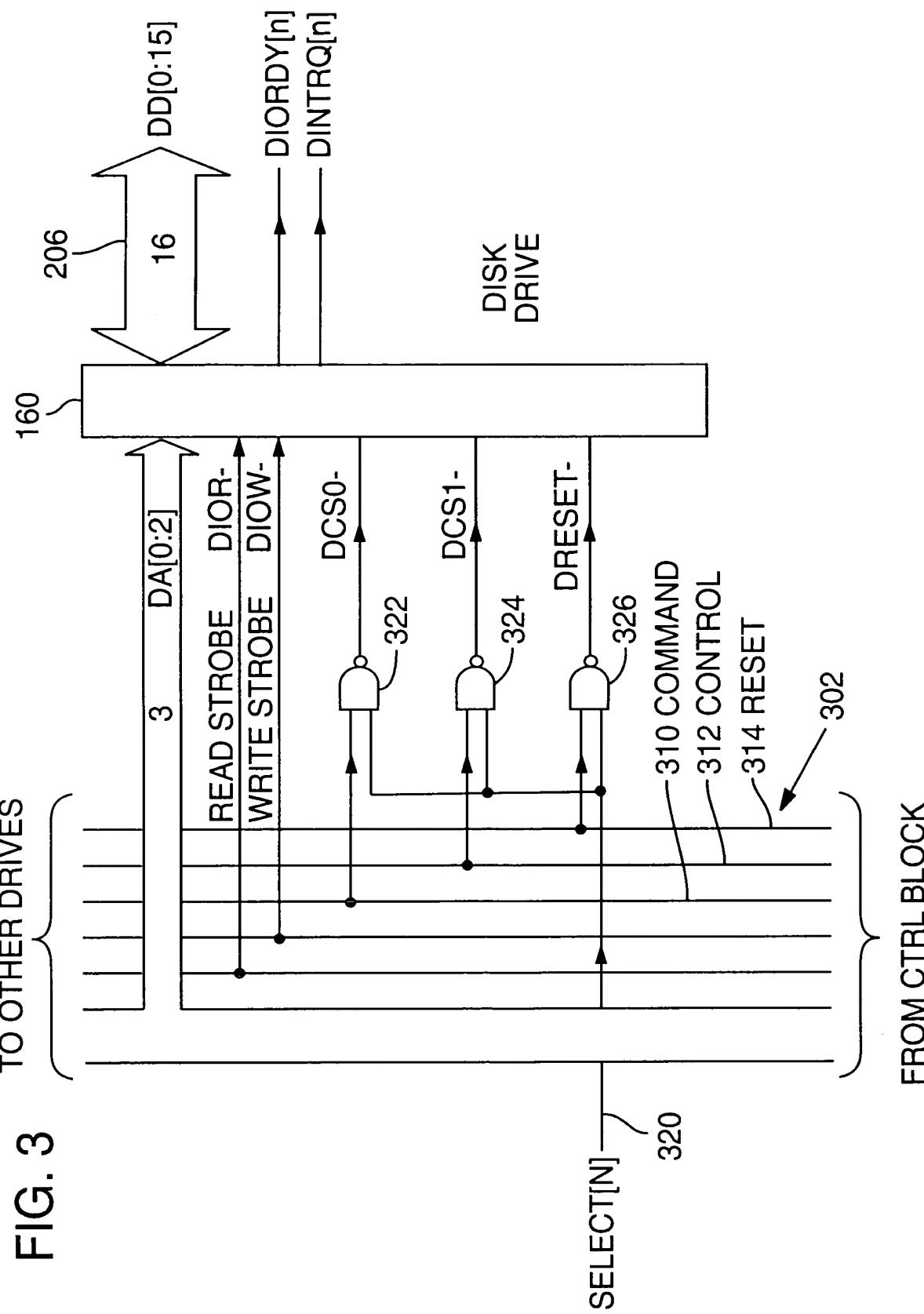


FIG. 2

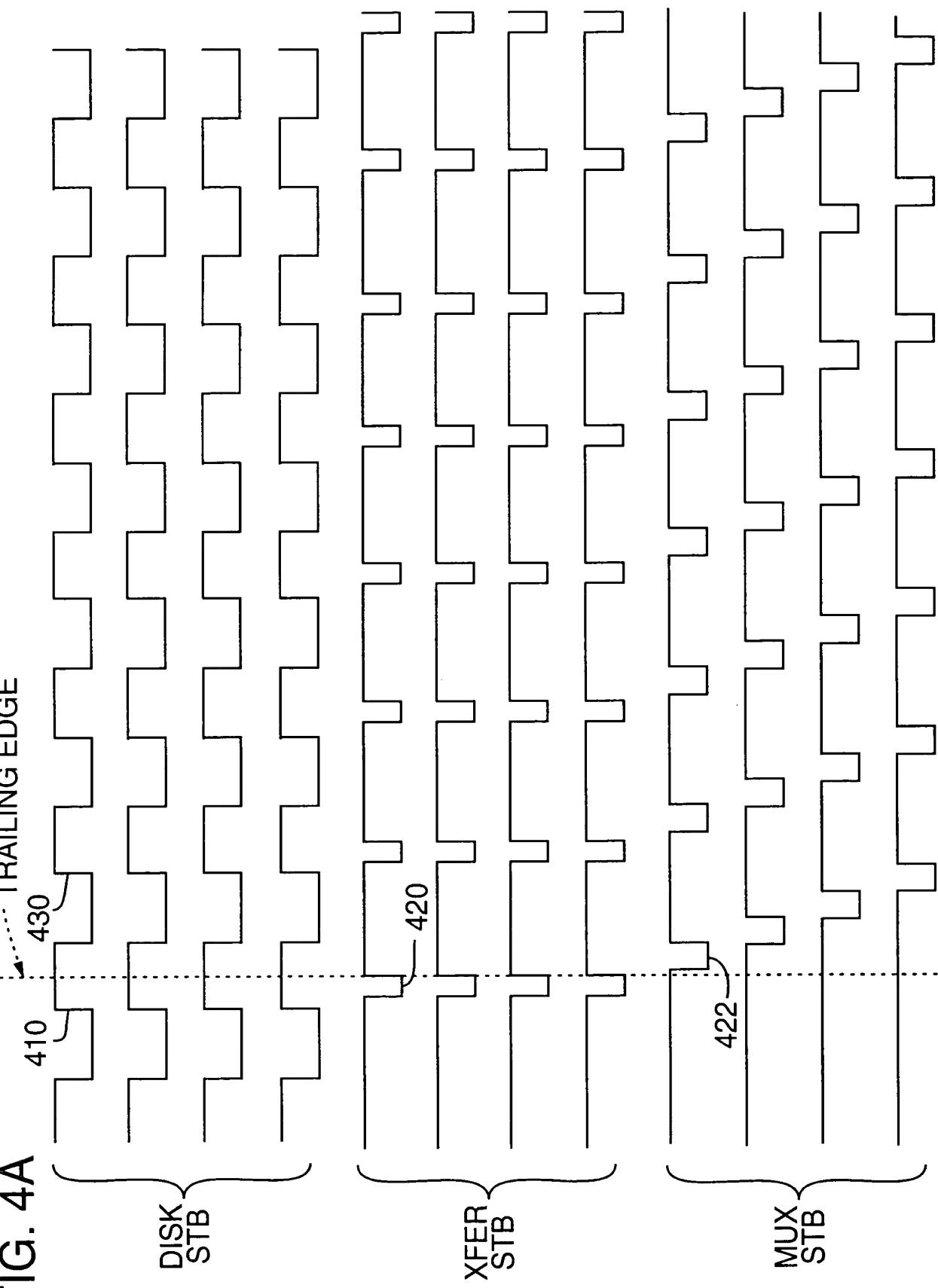


APPROVED BY DRAFTSMAN	O.G. FIG. 7
	CLASS 710 SUBCLASS 61

FIG. 3



The diagram shows a cross-section of an airfoil at the trailing edge. The airfoil has a concave upper surface and a convex lower surface. A dashed line extends from the trailing edge towards the top left, labeled '... TRAILING EDGE'. The number '430' is written below the airfoil.



APPROVED	O.G. FIG.	7
BY	CLASS	SUBCLASS
DRAFTSMAN	710	61

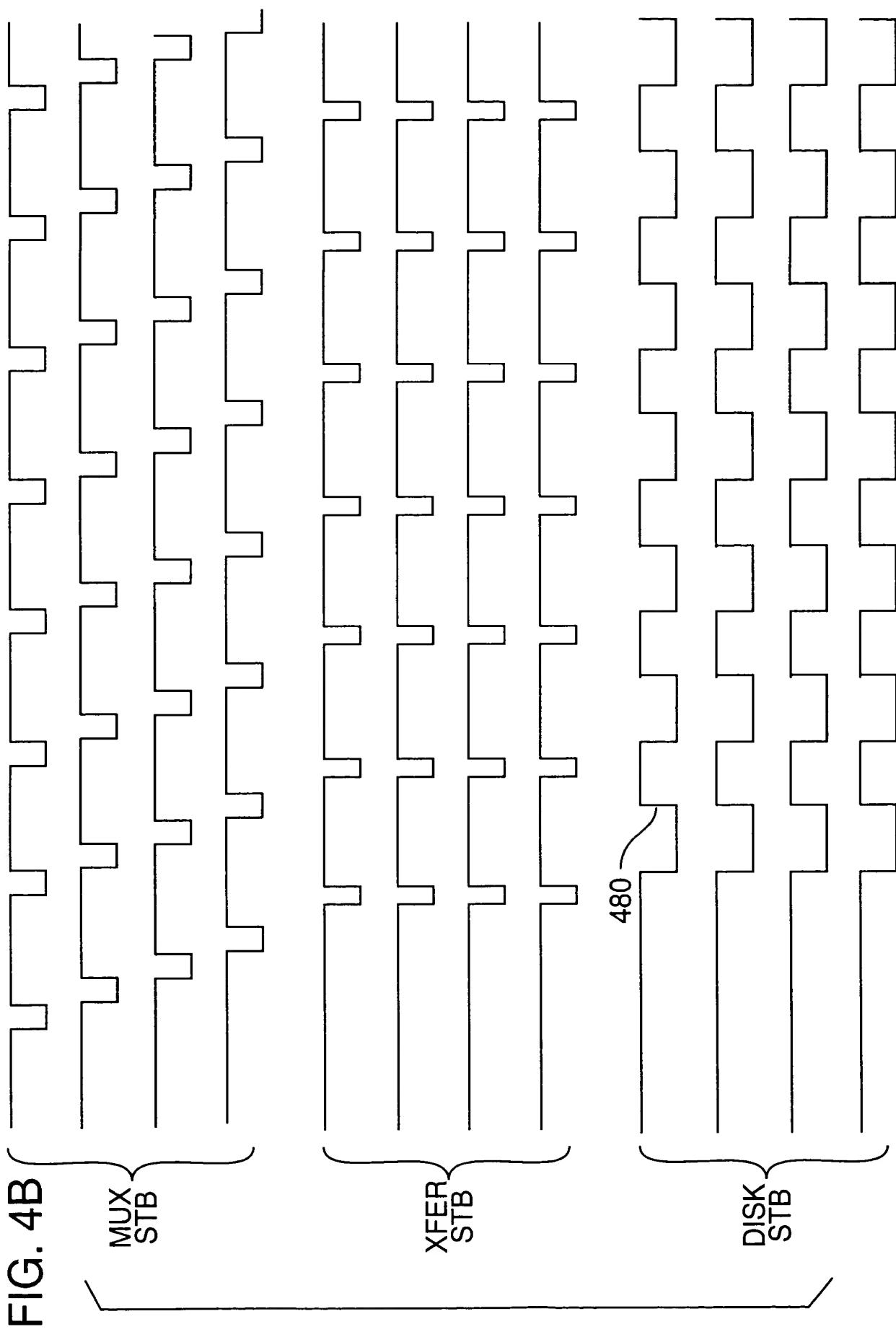


FIG. 5

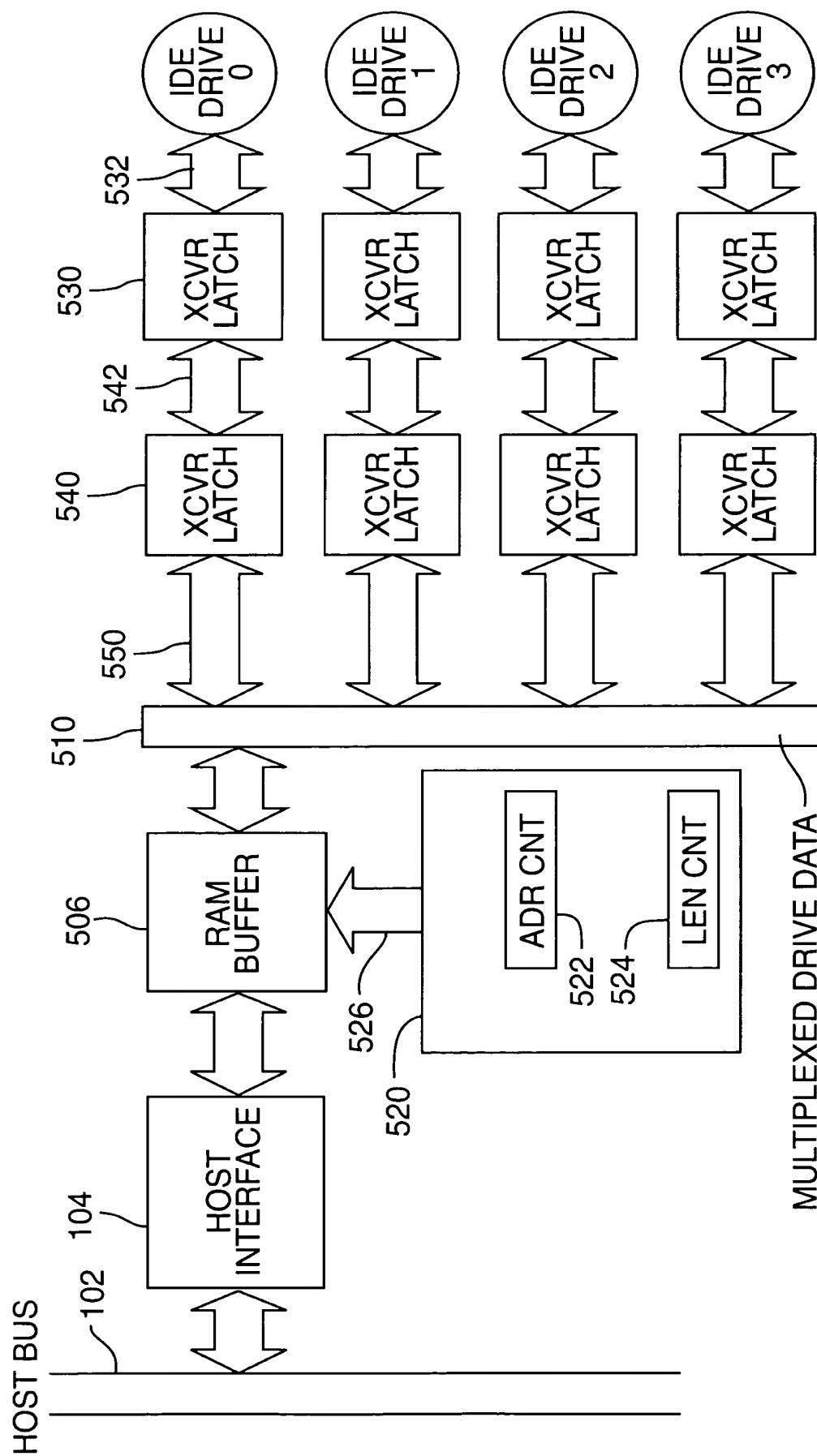
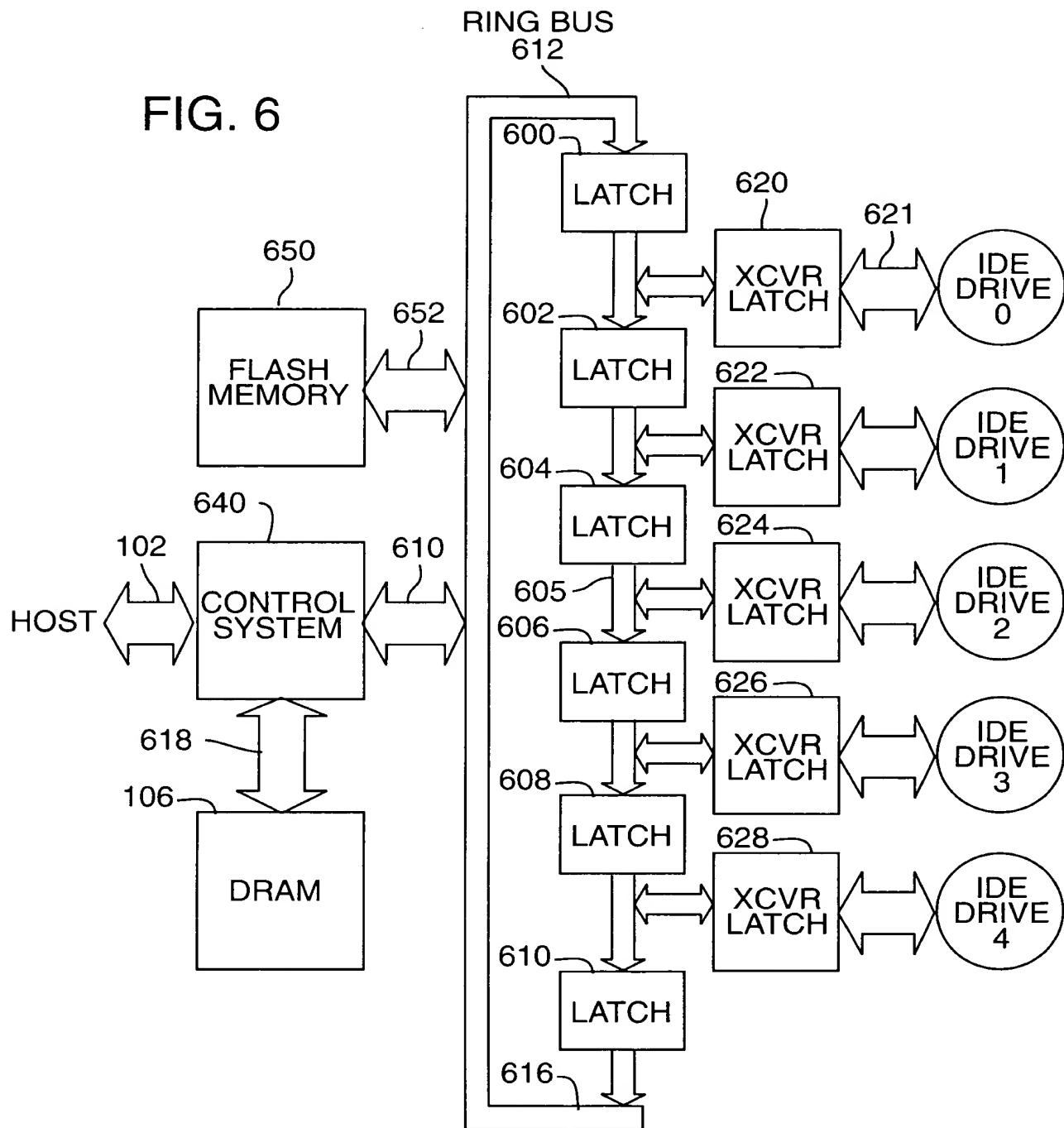


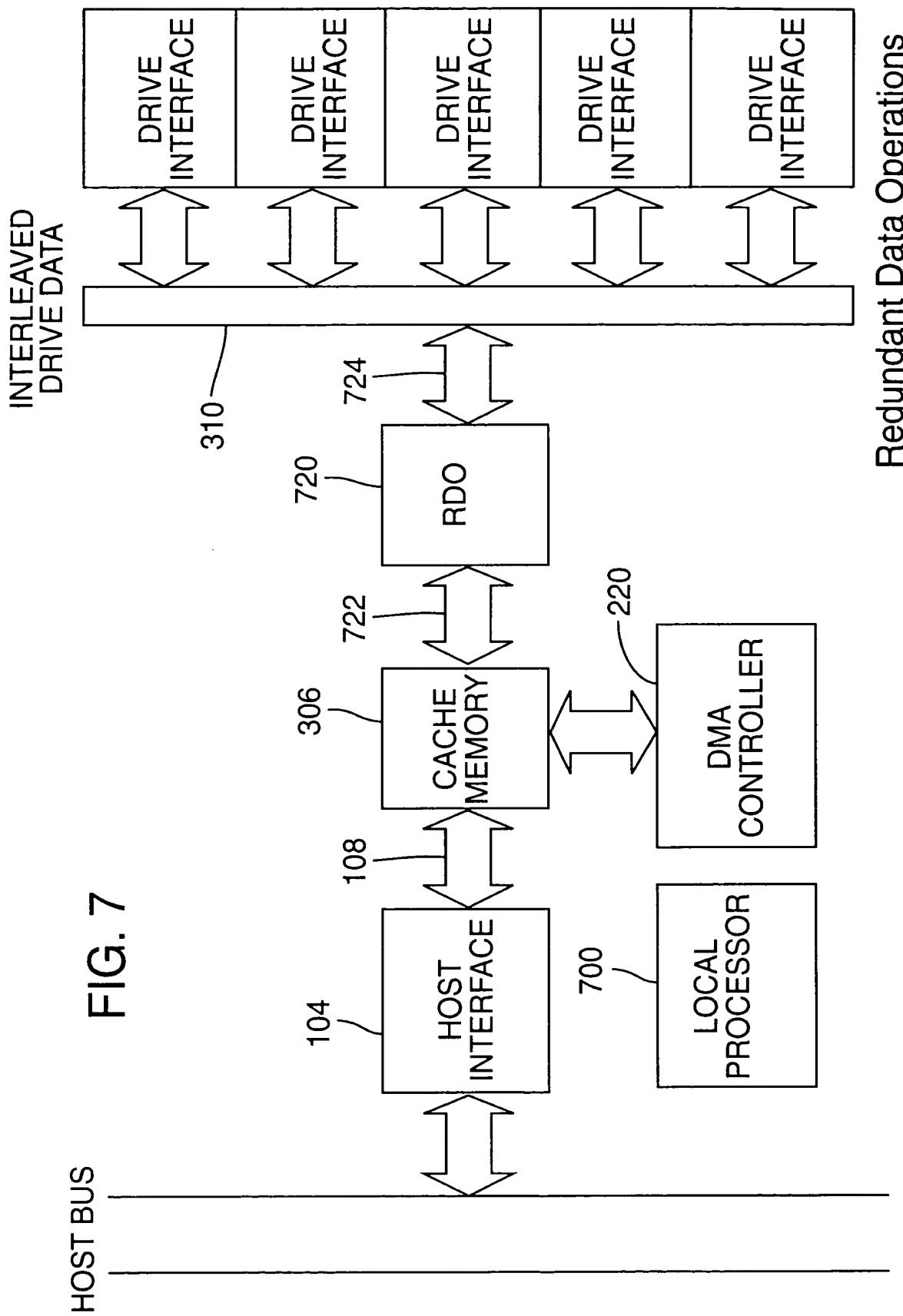
FIG. 6



APPROVED	O.G. FIG.	7
BY	CLASS	710
DRAFTSMAN	SUBCLASS	61

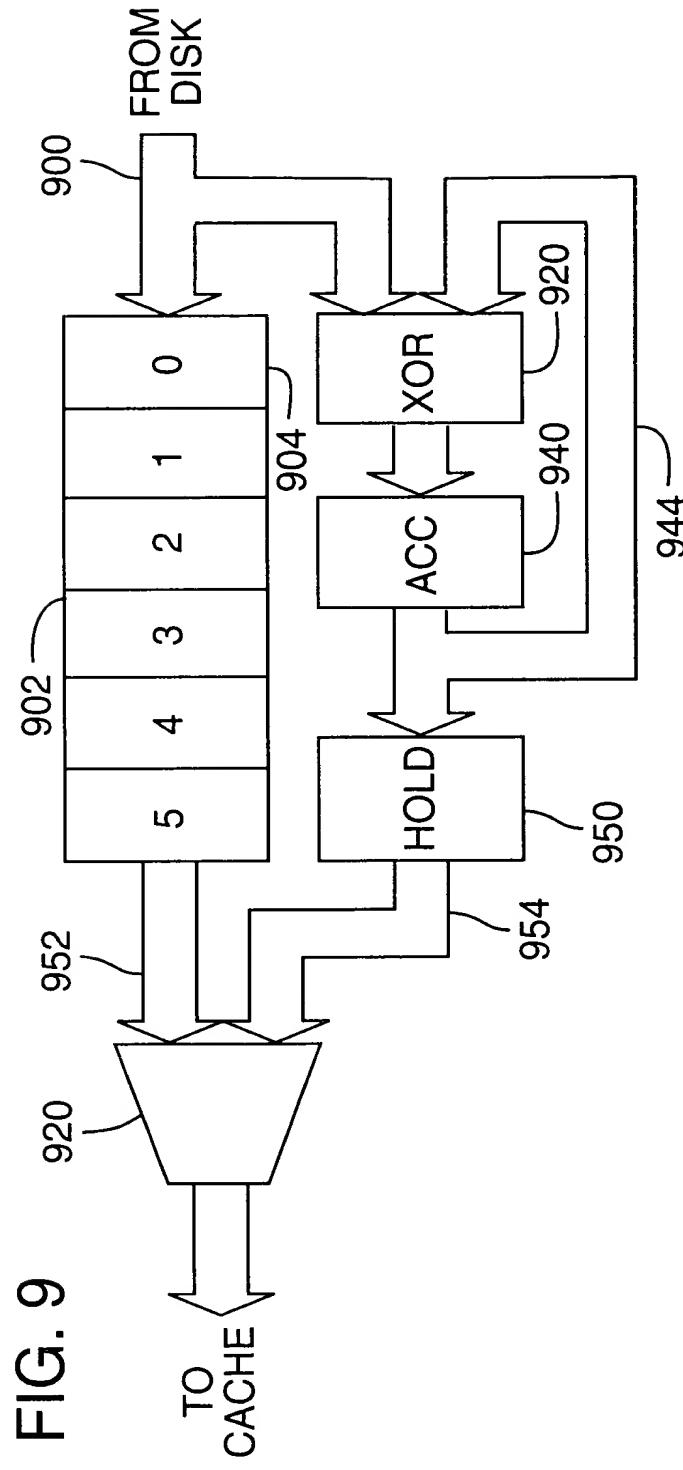
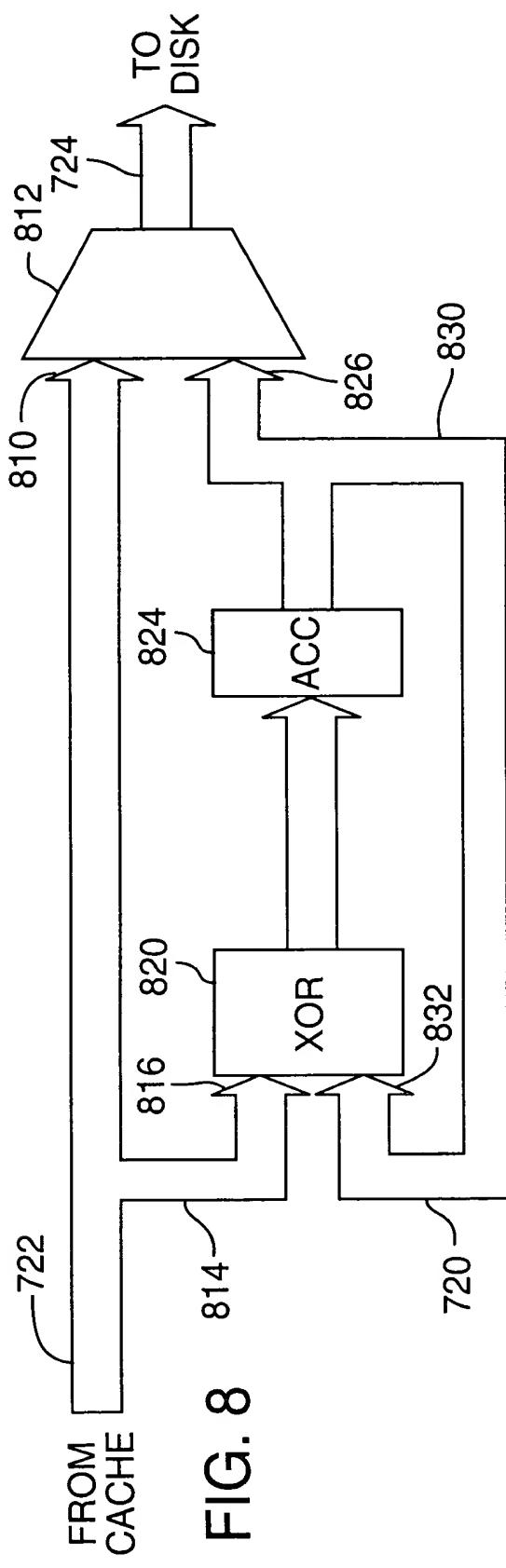
## SYNCHRONOUS DATA TRANSFER

FIG. 7



Redundant Data Operations

APPROVED BY DRAFTSMAN	O.G. FIG.
	CLASS      SUBCLASS



APPROVED BY DRAFTSMAN	O.G. FIG.
	CLASS      SUBCLASS

FIG. 10

DISK READ - NO CORRECTION

State	INPUT	ACCUMULATOR(940)		HOLD		PIPELINE(902)		OUTPUT
		FUNCTION	CONTENTS	LATCH	A0	B0	C0	
0	A0	LOAD	A0		A0			
1	B0	XOR	A0+B0		B0	A0		
2	C0	XOR	A0+B0+C0		C0	B0	A0	
3	D0	XOR	A0+B0+C0+D0		D0	C0	B0	A0
4	E0	XOR	A0+B0+C0+D0+E0		E0	D0	C0	B0
0	A1	LOAD	A1	A0+B0+C0+D0+E0	A1	E0	D0	C0
1	B1	XOR	A1+B1	A0+B0+C0+D0+E0	B1	A1	E0	D0
2	C1	XOR	A1+B1+C1	A0+B0+C0+D0+E0	C1	B1	A1	E0
3	D1	XOR	A1+B1+C1+D1	A0+B0+C0+D0+E0	D1	C1	B1	A1
4	E1	XOR	A1+B1+C1+D1+E1	A0+B0+C0+D0+E0	E1	D1	C1	B1
0				A1+B1+C1+D1+E1	E1	D1	C1	A1
1				A1+B1+C1+D1+E1	E1	D1	C1	B1
2				A1+B1+C1+D1+E1	E1	D1	C1	<b>B1</b>
3				A1+B1+C1+D1+E1	E1	D1	C1	C1
4				A1+B1+C1+D1+E1	E1	D1	C1	D1

APPROVED BY DRAFTSMAN	O.G. FIG.
	CLASS      SUBCLASS

**FIG. 11**

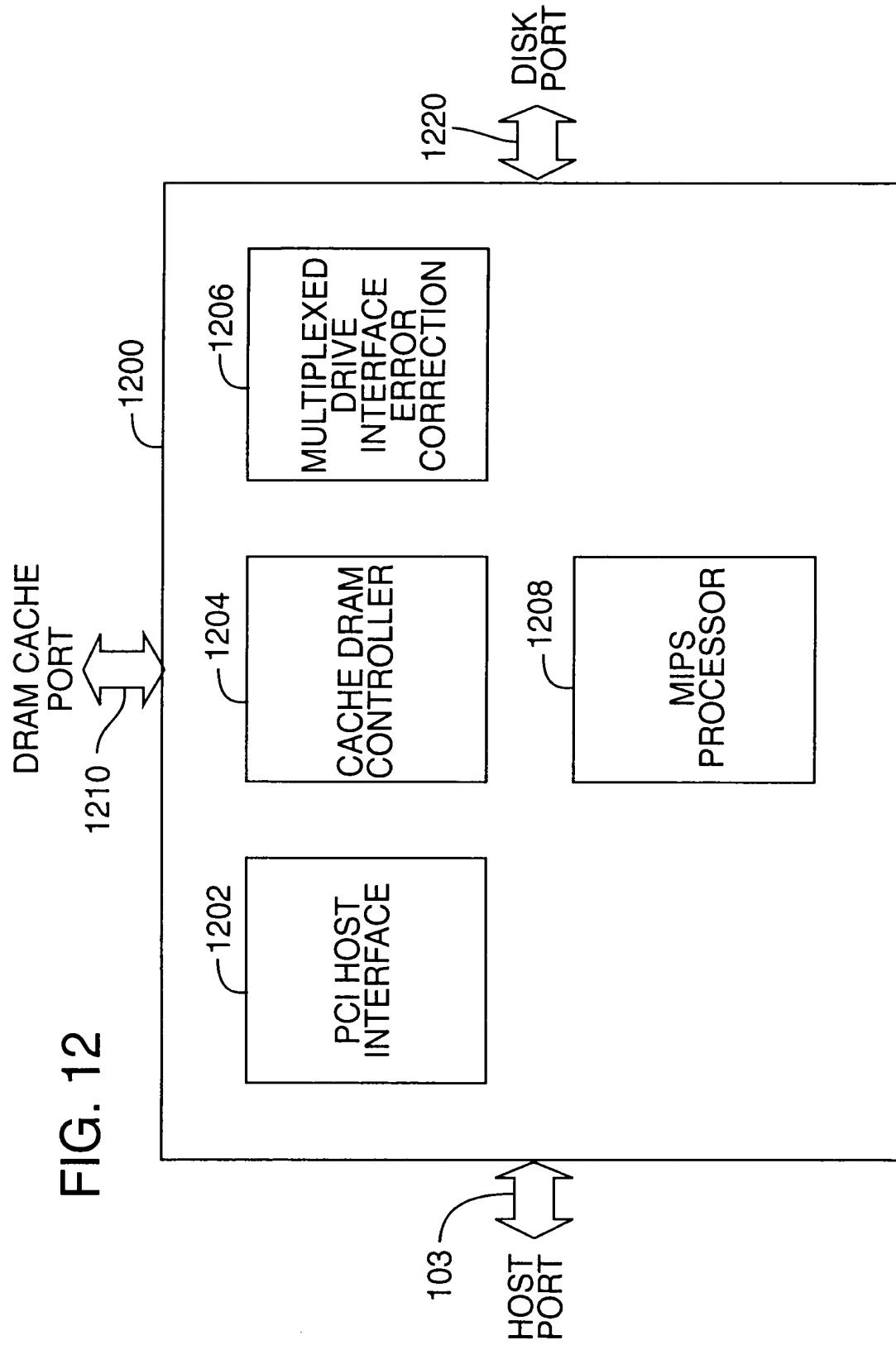
**DISK READ - WITH CORRECTION**

State	INPUT FUNCT	ACCUMULATOR(940) CONTENTS	HOLD LATCH	PIPELINE(902)		OUTPUT
				A0	(xxx) A0	
0	A0	LOAD A0		C0	(xxx) A0	
1	(xxx)	HOLD A0		D0	(xxx) A0	
2	C0	XOR A0+C0		E0	(xxx) A0	
3	D0	XOR A0+C0+D0		A0+C0+D0+E0	(xxx) A0	
4	E0	XOR A0+C0+D0+E0		A1	(xxx) A0	
0	A1	LOAD A1		A0+C0+D0+E0	A1	(xxx) A0
1	(xxx)	HOLD A1		A0+C0+D0+E0	(xxx) A1	(xxx) A0
2	C1	XOR A1+C1		A0+C0+D0+E0	C1	(xxx) A1
3	D1	XOR A1+C1+D1		A0+C0+D0+E0	D1	(xxx) A1
4	E1	XOR A1+C1+D1+E1		A0+C0+D0+E0	E1	D1
0				A1+C1+D1+E1	E1	C1
1				A1+C1+D1+E1	E1	D1
2				A1+C1+D1+E1	E1	C1
3				A1+C1+D1+E1	E1	D1
4				A1+C1+D1+E1	E1	D1

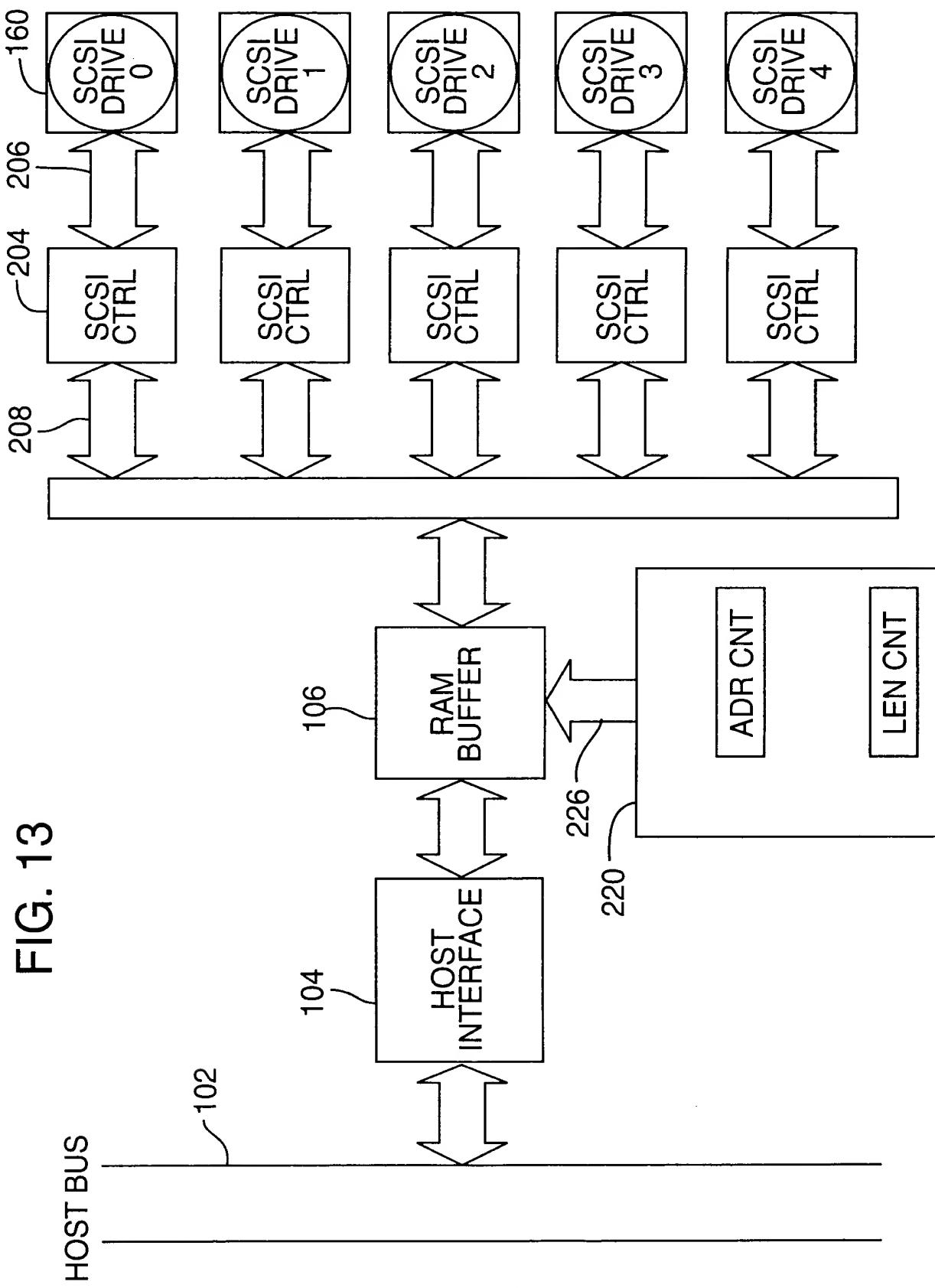
APPROVED	O.G. FIG.
BY	
DRAFTSMAN	CLASS      SUBCLASS

DISK ARRAY CONTROLLER CHIP

FIG. 12



APPROVED	O.G. FIG.
BY	
DRAFTSMAN	



APPROVED	O.G. FIG.
BY	
DRAFTSMAN	

